

Pinxu Wang

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Education

University of Illinois at Urbana-Champaign (UIUC)

Champaign IL, United States

Master of Engineering in Electrical and Computer Engineering

Aug 2024 Dec 2026

- Course: Computer Organization and Design, Digital System Lab (FPGA Development), VLSI Design

University of Electronic Science and Technology of China (UESTC)

Chengdu, China

B.S. in Microelectronics Science and Engineering

Aug 2019 May 2023

- Course: Analog Integrated Circuit Principles, Semiconductor Physics, IC Manufacturing Processes, Digital Integrated Circuit Principles

Skills and Software

- **HDL & Modeling:** SystemVerilog (RTL Design & TB), Verilog, C-Model (Behavioral Modeling), Gem5 (Arch. Simulation)
- **Verification:** UVM, Coverage-driven Verification, VIP Configuration, RVFI
- **EDA Tools & Flows:** Synopsys VCS/Verdi, Design Compiler, Spyglass (Lint/CDC), PrimeTime, Calibre(DRC/LVS)
- **Infrastructure & Tools:** Git, JIRA, Jenkins, Bazel, Makefile, AI: (Claude Code CLI, Cursor), LLM

Intern Experience

Digital IC Verification Engineer Intern | Enrigin Technology

Shanghai, China

AXI Address Mapping & Hash Routing Module Verification

Feb 2025 Aug 2025

- Authored test plans for Address Mapping, Hash Routing, Burst Clipping; resolved SoC spec gaps via design review.
- Built macro/plusarg-driven UVM env on AXI VIP for cross-IP and multi-instance reuse.
- Owned ID Remap/Reorder verification after AXI ID width 9→12-bit extension; covered all-identical/all-unique/random-outstanding ID scenarios; root-caused a CAM aliasing corner case.
- Built scoreboard with bit-accurate reference models for NUMA hash routing and 512B boundary clipping (AxSize=0..7, unaligned addresses, narrow transfers); hit 100% code + functional coverage for module signoff.

Projects

NPU Chip Design & Verification | 22nm TSMC CNN Accelerator (Tape-out, Silicon-Validated)

Feb 2026 – now

Design (co-developed): 22nm TSMC CNN inference NPU for MNIST/CIFAR-10; FP16 datapath, 1Mb SRAM, AXI/APB/SPI bus, 400 MHz, 4 async clocks.

- Co-designed FP16 MAC datapath (6-ch/16-ch Conv + max-pool + 3-stage FC) and weight/activation SRAM layout for bandwidth/area tradeoff; integrated INT8→FP16 dequant frontend.
- Contributed to AXI/APB/SPI bus integration and 4-domain CDC (sync_bit / async-FIFO); reviewed RTL for clock-mux, reset sync, PLL bring-up.

Verification (owned): Full-chip pre-silicon UVM with RAL, scoreboard, image UVC, coverage closure.

- Built full-chip UVM env on Synopsys AXI/SPI VIP with custom image UVC (RGB raster) and RAL via SPI→APB reg_adapter.
- Authored vplan + UVM sequences for register RW, MNIST/CIFAR-10 golden inference, multi-frame switching, SPI SRAM readback, PLL bring-up.
- Built bit-true scoreboard vs SW golden: FP16 dequant, 6-ch/16-ch MAC, max-pool, 3-stage FC.
- Closed CDC sign-off across 4 async clocks; ran VCS/Verdi regression + coverage via regress.py with mem_load backdoor.

Single-Issue RISC-V Out-of-Order RV32IM Processor

Sep 2024 – Dec 2024

Overview: Single-issue OoO RV32IM core with Tomasulo 5-stage pipeline, Harvard cache, and BTB+RAT BP

- Implemented Tomasulo register renaming + RVS for dynamic scheduling and data hazard resolution.
- Designed Harvard arch with 4-way set-associative I/D-Cache, write-back + write-allocate, PLRU replacement.
- BTB + RAT branch predictor: 88% accuracy, ~18% IPC improvement.
- Top-Down analysis with performance counters to identify and optimize load / branch latency bottlenecks.